Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1 (original): A method for fabricating a gate electrode, wherein said method comprising:

providing a substrate;

forming a first barrier layer on said substrate;

forming a dielectric layer with a high dielectric constant on said first barrier layer;

performing a post-deposition annealing to said dielectric layer;

depositing a second barrier layer on said dielectric layer;

forming a metal gate layer on said barrier layer; and

removing a portion of said metal gate layer, said second barrier layer, said dielectric layer, and said first barrier layer to form a gate electrode on said substrate.

Claim 2 (currently amended): The method according to claim 1, wherein the ~~steps~~ step of forming said first barrier layer comprises a first nitrogen-containing rapid thermal process.

Claim 3 (original): The method according to claim 2, wherein said first nitrogen-containing rapid thermal process further comprising an ammonia rapid thermal process.

Claim 4 (original): The method according to claim 2, wherein the temperature of said first nitrogen-containing rapid thermal process is between 600 °C to 750 °C.

Claim 5 (original): The method according to claim 2, wherein the duration of said first nitrogen-containing rapid thermal process is between the 10 to 20 minutes.

Claim 6 (original): The method according to claim 1, wherein the material of said first barrier layer is selected from the group consisting of

silicon dioxide (SiO_2), silicon nitride (SiN_x), and silicon oxynitride (SiON).

Claim 7 (original): The method according to claim 1, wherein the material of said dielectric layer is selected from the group consisting of zirconium dioxide (ZrO_2), hafnium dioxide (HfO_2), zirconium silicates (Zr-silicates), hafnium silicates (Hf-silicates), La_2O_3 (lanthanum oxide), Y_2O_3 (yttrium oxide), and Al-doped Zr-silicate ($(Al_2O_3)(ZrO_2)_x(SiO_2)_{1-x-y}$).

Claim 8 (original): The method according to claim 1, wherein said dielectric layer with said high dielectric constant is about 10.

Claim 9 (original): The method according to claim 1, wherein the steps of said fabricating said gate electrode on said substrate further comprising:

performing a post-deposition annealing to said dielectric layer;

depositing a second barrier layer on said dielectric layer;

depositing a metal gate layer on said second barrier layer;

forming a photoresist layer on said metal gate layer; and

sequentially etching said metal gate layer, said second barrier layer,

said dielectric layer, and said first barrier layer to form a gate electrode on said substrate.

Claim 10 (original): The method according to claim 1, wherein the temperature of said post-deposition annealing is between 700 °C to 900 °C.

Claim 11(original): The method according to claim 1, wherein the duration of said post-deposition annealing is between 20 to 45 minutes.

Claim 12 (original): The method according to claim 1, wherein the material of said second barrier layer is selected from the group consisting of silicon dioxide (SiO_2), silicon nitride (SiN_x), and silicon oxynitride (SiON).

Claim 13 (original): The method according to claim 1, further comprising a second nitrogen-containing rapid thermal process treatment to treat said gate electrode.

Claim 14 (currently amended): The method according to claim ~~9~~13, wherein said second nitrogen-containing rapid thermal process comprises an

ammonia rapid thermal process.

Claim 15 (original): The method according to claim 1, wherein the material of said metal gate layer is selected from the group consisting of tantalum (Ta), tantalum nitride (TaN_x), and $TaRu_xN_y$ (tantalum-ruthenium-nitrogen).

Claim 16 (original): A method for fabricating a gate electrode, said method comprising:

providing a substrate;

treating said substrate by a first nitrogen-containing rapid thermal process to form a first barrier layer thereon;

depositing a dielectric layer with a high dielectric constant on said first barrier layer;

performing a post-deposition annealing process on said dielectric layer;

forming a second barrier layer on said dielectric layer;

forming a metal gate layer on said second barrier layer;

forming a photoresist layer on said metal gate layer;

sequentially etching said metal gate layer, said second barrier layer, said

dielectric layer, and said first barrier layer to form a gate electrode on said substrate; and

performing a second nitrogen-containing rapid thermal process on said gate electrode.

Claim 17 (original): The method according to claim 16, wherein said first nitrogen-containing rapid thermal process further comprising an ammonia rapid thermal process.

Claim 18 (currently amended): The method according to claim 16, wherein the temperature of said first ~~ammonia~~ nitrogen-containing rapid thermal process (NH_3 RTP) is between 600°C to 750°C.

Claim 19 (original): The method according to claim 16, wherein the duration of said first nitrogen-containing rapid thermal process is between 10 to 20 minutes.

Claim 20 (original): The method according to claim 16, wherein the material of said first barrier layer is selected from the group consisting of

silicon dioxide (SiO_2), silicon nitride (SiN_x), and SiON (silicon oxynitride).

Claim 21 (original): The method according to claim 16, wherein said dielectric layer is selected from the group consisting of zirconium dioxide (ZrO_2), hafnium dioxide (HfO_2), zirconium silicates (Zr-silicates), hafnium silicates (Hf-silicates, La_2O_3 (lanthanum oxide), Y_2O_3 (yttrium oxide), and Al-doped Zr-silicate ($(Al_2O_3)(ZrO_2)_x(SiO_2)_{1-x-y}$).

Claim 22 (original): The method according to claim 16, wherein said dielectric layer with said high dielectric constant is about 10.

Claim 23 (original): The method according to claim 16, wherein said performing post-deposition annealing comprises a post-deposition annealing in nitrogen gas.

Claim 24 (original): The method according to claim 23, wherein the temperature of said post-deposition annealing is between 700 °C to 900 °C.

Claim 25 (original): The method according to claim 23, wherein the

duration of said post-deposition annealing is between 20 to 45 minutes.

Claim 26 (original): The method according to claim 16, wherein the material of said second barrier layer is selected from the group consisting of silicon dioxide (SiO_2), silicon nitride (SiN_x), and SiON (silicon oxynitride).

Claim 27 (original): The method according to claim 16, wherein the material of said metal gate layer is selected from the group consisting of tantalum (Ta), tantalum nitride (TaN_x), and $TaRu_xN_y$ (tantalum-ruthenium-nitrogen).

Claim 28 (original): The method according to claim 16, wherein said second nitrogen-containing rapid thermal process further comprising an ammonia rapid thermal process.

Claim 29 (original): A method for forming the gate electrode, said method comprising:

providing a substrate;

treating said substrate by a first ammonia rapid thermal process (NH_3

RTP) to form a first barrier layer on said substrate;

chemical vapor depositing a dielectric layer on said first barrier layer, wherein the dielectric constant of said dielectric layer is about 10;

performing a post-deposition annealing in nitrogen gas on said dielectric layer;

chemical vapor depositing a second barrier layer on said dielectric layer;

chemical vapor depositing a metal gate layer on said second barrier layer;

forming a photoresist layer on said metal gate layer;

sequentially etching said metal gate layer, said second barrier layer, said dielectric layer, and said first barrier layer to form a gate electrode on said substrate; and

performing a second ammonia rapid thermal process (NH_3 RTP) on said gate electrode to form a surface inhibition layer on the sidewall of said gate electrode.

Claim 30 (original): The method according to claim 29, wherein the temperature of said first ammonia rapid thermal process (NH_3 RTP) is

between 600 °C to 750 °C.

Claim 31 (original): The method according to claim 29, wherein the duration of said first ammonia rapid thermal process (NH_3 RTP) is between 10 to 20 minutes.

Claim 32 (original): The method according to claim 29, wherein material of said first barrier layer is selected from the group consisting of silicon dioxide (SiO_2), silicon nitride (SiN_x), and silicon oxynitride (SiON).

Claim 33 (original): The method according to claim 29, wherein said dielectric layer is selected from the group consisting of zirconium dioxide (ZrO_2), hafnium dioxide (HfO_2), zirconium silicates (Zr-silicates), and hafnium silicates (Hf-silicates), and La_2O_3 (lanthanum oxide), Y_2O_3 (yttrium oxide), and Al-doped Zr-silicate ($(Al_2O_3)(ZrO_2)_x(SiO_2)_{1-x-y}$).

Claim 34 (original): The method according to claim 29, wherein the temperature of said post-deposition annealing is between 700 °C to 900 °C.

Claim 35 (original): The method according to claim 29, wherein the duration of said post-deposition annealing is between 20 to 45 minutes.

Claim 36 (original): The method according to claim 29, wherein the material of said second barrier layer is selected from the group consisting of silicon dioxide (SiO_2), silicon nitride (SiN_x), and SiON (silicon oxynitride).

Claim 37 (original): The method according to claim 29, wherein the temperature of said second ammonia rapid thermal process is about 600 □.

Claim 38 (original): The method according to claim 29, wherein the duration of said second ammonia rapid thermal process is about 20 minutes.

Claim 39 (original): The method according to claim 29, wherein said surface inhibition layer comprises TaN_x.